REMARKS

Claims 1-27 are pending. Claim 7 is objected to because of informalities. Claim 7 has been amended to correct informalities. The Examiner rejected claims 1-27 including independent claims 1, 11, and 21 under 35 U.S.C. 120(e) as being anticipated by Oh (6,996,016 B2).

Oh describes "a system 100 using a burst PSRAM device 104. In one embodiment, the system 100 generally comprises a system controller 102, a memory 104, an address/command (i.e., system) bus 106, and a data (i.e., DQ) bus 108. The memory 104 may comprise one or more component memories (discussed below in reference to FIG. 2), where each component memory is coupled to the buses 106 and 108. The system bus 106 may comprise unidirectional and bi-directional transmission lines, while the DQ bus includes bi-directional transmission lines. The system controller 102 is typically coupled to a processor of an external electronic device 110 (e.g., computer, cell phone, and the like) using an application-specific interface 112.

In one embodiment of the invention, the system bus 106 comprises a bi-directional line 114 (shown in phantom) that transmits a WAIT_DQS signal and a plurality unidirectional transmission lines propagating conventional control and command signals. Such conventional control and command signals comprise, among other such signals, a Clock (CLK) signal, an Address (e.g., 21-bit address word A20-A0) signal, an Address Valid (ADV) signal, a Write Enable (WE) signal, and a Chip Select (CS) signal (all discussed below in reference to FIGS. 3-7)." (column 4, lines 1-24)

The Examiner relies on this description and associated Figure 1 to teach the elements of the claims. It is acknowledged that Figure 1 and the corresponding text do describe a processor 110 and a memory 104 and buses 106 and 108. However, Oh is not believed to teach or suggest receiving information about the primary component and the second component and generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components.

The Examiner may attempt to argue that receiving this information and generating the interconnection module are inherent in Oh. The Applicants respectfully disagree. The interconnection module in Oh may be standard bus used to connect components. No interconnection module has to be generated. In many instances, a standard bus is used as an interconnect. However, the techniques of the present invention recite "receiving information about a primary component and a secondary component" and "generating an interconnection module coupling the primary component to the secondary component." Oh does not teach or suggest any receiving information about a first primary component or receiving any information about a first secondary component. Oh furthermore does not teach or suggest "generating an interconnection module coupling the primary component to the secondary component, the interconnection module including data, address, and control lines, wherein the interconnection module supports a system having both fixed latency and variable latency components."

Claim 11 recites an input interface configured to receive information associated with a primary component and information associated with a secondary component ... and a processor configured to generate interconnection circuitry coupling the primary component to the secondary component, the interconnection module including data, address, and control lines for the programmable chip. Oh does not teach or suggest an input interface or any processor configured to perform the above noted elements. Oh only describes a processor connected to a memory over a bus.

CONCLUSION

In light of the above remarks relating to the independent claims, the remaining dependent claims are believed allowable for at least the reasons noted above. Applicants believe that all pending claims are allowable and respectfully request a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
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